CLAIMS

What is claimed is:

1. A method of making a semiconductor device, the method comprising:

providing a semiconductor substrate having a patterned interconnect layer formed thereon;

depositing a first dielectric material over the patterned interconnect layer;

depositing a first electrode material over the first dielectric material;

depositing a second dielectric material over the first electrode material;

depositing a second electrode material over the second dielectric material;

patterning the second electrode material to form a top electrode of a first capacitor; and

patterning the first electrode material to form a top electrode of a second capacitor, to form an electrode of the first capacitor, and to define a resistor.

2. The method of claim 1 wherein:

the patterned interconnect layer forms a bottom electrode of the second capacitor and is absent from the first capacitor.

3. The method of claim 1 wherein:

the patterned interconnect layer forms a bottom electrode of the first capacitor and a bottom electrode of the second capacitor.

4. The method of claim 3 wherein:

the electrode of the first capacitor comprises a middle electrode of the first capacitor; and

the middle electrode of the first capacitor is located between the top electrode of the first capacitor and the bottom electrode of the first capacitor.

5. The method of claim 4 further comprising:

forming electrical contacts coupled to each of the top, middle, and bottom electrodes of the first capacitor; and

forming electrical contacts coupled to each of the top and bottom electrodes of the second capacitor,

wherein:

forming the electrical contacts comprises:

forming each of the electrical contacts to each of the top, middle, and bottom electrodes of the first capacitor and to each of the top and bottom electrodes of the second capacitor substantially simultaneously with each other.

6. The method of claim 4 further comprising:

forming electrical contacts coupled to each of the top and middle electrodes of the first capacitor, but not to the bottom electrode of the first capacitor; and

forming an electrical contact coupled to at least the top electrode of the second capacitor.

7. The method of claim 6 wherein:

forming the electrical contacts comprises:

forming each of the electrical contacts to each of the top and middle electrodes of the first capacitor and to each of the top and bottom electrodes of the second capacitor substantially simultaneously with each other.

8. The method of claim 1 further comprising:

after depositing the first dielectric material, patterning the first dielectric material to form an opening that exposes a portion of the patterned interconnect layer,

wherein:

depositing the first electrode material includes depositing a portion of the first electrode material in the opening such that the portion of the first electrode material is in contact with the portion of the patterned interconnect layer.

9. The method of claim 1 wherein:

the first dielectric material comprises silicon nitride; and

the second dielectric material comprises a material having an effective dielectric constant greater than approximately eight.

10. The method of claim 9 wherein:

the second dielectric material comprises:

a first layer of hafnium oxide;

a layer of tantalum oxide above the first layer of hafnium oxide; and

a second layer of hafnium oxide above the layer of tantalum oxide.

11. The method of claim 1 wherein:

the patterned interconnect layer comprises damascene copper; and

the first and second electrode materials comprise tantalum nitride.

12. The method of claim 1 further comprising:

forming electrical contacts coupled to the resistor.

13. The method of claim 1 wherein:

the first dielectric material comprises silicon nitride;

the second dielectric material comprises:

a first layer of hafnium oxide;

a layer of tantalum oxide above the first layer of hafnium oxide; and

a second layer of hafnium oxide above the layer of tantalum oxide;

the patterned interconnect layer comprises damascene copper; and

the first and second electrode materials comprise tantalum nitride.

14. A semiconductor device comprising:

a semiconductor substrate;

a patterned interconnect layer above the semiconductor substrate;

a first capacitor above the patterned interconnect layer;

a second capacitor above the patterned interconnect layer; and

a resistor above the patterned interconnect layer,

wherein:

the first capacitor comprises a layer of electrode material and further comprises a first number of dielectric layers;

the second capacitor comprises the layer of electrode material and further comprises a second number of dielectric layers; and

the first number of dielectric layers is greater than the second number of dielectric layers such that the first capacitor has a higher capacitance per unit area than does the second capacitor.

15. The semiconductor device of claim 14 wherein:

at least one of the dielectric layers of the first capacitor comprises a material that is different from a material of at least one of the dielectric layers of the second capacitor.

16. The semiconductor device of claim 15 wherein:

the first number of dielectric layers comprises a first dielectric material and a second dielectric material;

the second number of dielectric layers comprises the first dielectric material;

the first dielectric material comprises silicon nitride;

the second dielectric material comprises a material having an effective dielectric constant greater than approximately eight; and

the layer of electrode material comprises tantalum nitride.

17. The semiconductor device of claim 16 wherein:

the second dielectric material comprises:

a first layer of hafnium oxide;

a layer of tantalum oxide above the first layer of hafnium oxide; and

a second layer of hafnium oxide above the layer of tantalum oxide.

18. A method of making a semiconductor device, the method comprising:

providing a semiconductor substrate having a patterned interconnect layer formed thereon, portions of the patterned interconnect layer defining a bottom electrode of a first capacitor and a bottom electrode of a second capacitor;

depositing a first dielectric material over the patterned interconnect layer;

patterning the first dielectric material to form an opening that exposes a portion of the patterned interconnect layer;

depositing a first electrode material over the first dielectric material and within the opening such that the first electrode material contacts the portion of the patterned interconnect layer;

depositing a second dielectric material over the first electrode material;

depositing a second electrode material over the second dielectric material;

patterning the second electrode material to form a top electrode of the first capacitor; and

patterning the first electrode material to form a top electrode of the second capacitor and a bottom electrode of the first capacitor.

19. The method of claim 18 wherein:

patterning the first electrode material further comprises forming a resistor.

20. The method of claim 18 wherein:

the first dielectric material comprises plasma enhanced nitride.

21. The method of claim 18 further comprising:

forming electrical contacts to each of the top and bottom electrodes of the first capacitor; and

forming electrical contacts to each of the top and bottom electrodes of the second capacitor,

wherein:

forming the electrical contacts comprises:

forming each of the electrical contacts to each of the top and bottom electrodes of the first capacitor and to each of the top and bottom electrodes of the second capacitor substantially simultaneously with each other.

22. The method of claim 21 further comprising:

forming electrical contacts coupled to the top electrode of the first capacitor but not to the bottom electrode of the first capacitor; and

forming an electrical contact coupled to at least the top electrode of the second capacitor.

23. The method of claim 18 wherein:

the first electrode material comprises tantalum nitride; and

the second dielectric material comprises a material having an effective dielectric constant greater than approximately eight.

24. The method of claim 23 wherein:

the second dielectric material comprises:

a first layer of hafnium oxide;

a layer of tantalum oxide above the first layer of hafnium oxide; and

a second layer of hafnium oxide above the layer of tantalum oxide.

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25. The method of claim 18 wherein:

patterning the first electrode material comprises defining a resistor; and

the method further comprises:

forming electrical contacts to the resistor.

26. A method of making a semiconductor device, the method comprising:

providing a semiconductor substrate having a patterned interconnect layer formed thereon;

depositing a first dielectric material over the patterned interconnect layer;

patterning the first dielectric material to form a first opening and a second opening in the first dielectric material;

depositing a first electrode material on the first dielectric material and in the first and second openings;

depositing a second dielectric material on the first electrode material;

depositing a second electrode material on the second dielectric material;

depositing a third dielectric material on the second electrode material;

depositing a third electrode material on the third dielectric material;

patterning the third electrode material to form a top electrode of a first capacitor;

patterning the third dielectric material and the second electrode material to form a middle electrode of the first capacitor and a top electrode of a second capacitor; and

patterning the second dielectric material and the first electrode material to form a bottom electrode of the first capacitor and a bottom electrode of the second capacitor.

27. The method of claim 26 further comprising:

forming electrical contacts to each of the top, middle, and bottom electrodes of the first capacitor; and

forming electrical contacts to each of the top and bottom electrodes of the second capacitor.

28. The method of claim 27 wherein:

forming the electrical contacts comprises:

forming each of the electrical contacts to each of the top and middle electrodes of the first capacitor and to each of the top and bottom electrodes of the second capacitor substantially simultaneously with each other.

29. The method of claim 26 wherein:

the first dielectric material comprises plasma enhanced nitride; and

the second dielectric material comprises a layer of tantalum oxide located between two layers of hafnium oxide.

30. The method of claim 26 wherein:

the first electrode material, the second electrode material, and the third electrode material comprise tantalum nitride; and

the patterned interconnect layer comprises damascene copper.

31. The method of claim 26 wherein:

patterning the first electrode material comprises defining a resistor; and

the method further comprises:

forming electrical contacts to the resistor.

32. A method of making a semiconductor device, the method comprising:

providing a semiconductor substrate having a patterned interconnect layer formed thereon;

depositing a first dielectric material over the patterned interconnect layer;

depositing a first electrode material over the first dielectric material;

depositing a second dielectric material over the first electrode material;

depositing a second electrode material over the second dielectric material;

patterning the second electrode material to form a top electrode of a first capacitor; and

patterning the first electrode material to form a top electrode of a second capacitor and an electrode of the first capacitor,

wherein:

the patterned interconnect layer forms a bottom electrode of the second capacitor and is absent from the first capacitor.